BE SEM - III (CBSGS) NOV-DEC-2016

Sub - CTL

24/12/16

QP Code : 545602

(3 Hours) **[Total Marks : 80**

N. B. : (1) Question No. 1 is **compulsory**.
(2) Attempt any **three** questions from the remaining **five**.
(3) **Figures** to the **right** indicate **full** marks.
(4) Use Smith chart for transmission line problem.
(5) Assume suitable data if required.

(a) In the network shown in fig. (1), find the voltages V_1 and V_2. 5

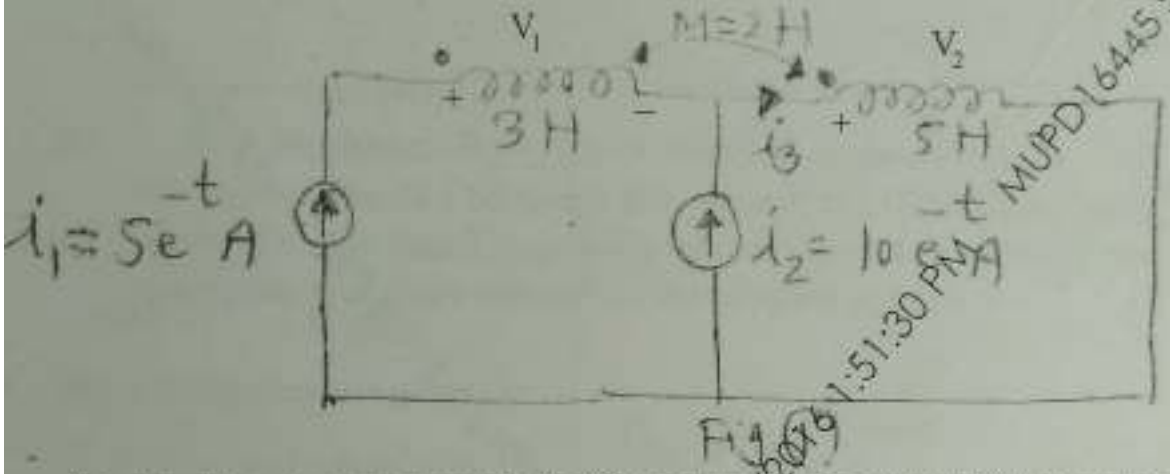


Fig (1)

(b) For the network shown in fig (2), determine the current i(t) when the switch is closed at t = 0 with zero initial conditions. 5

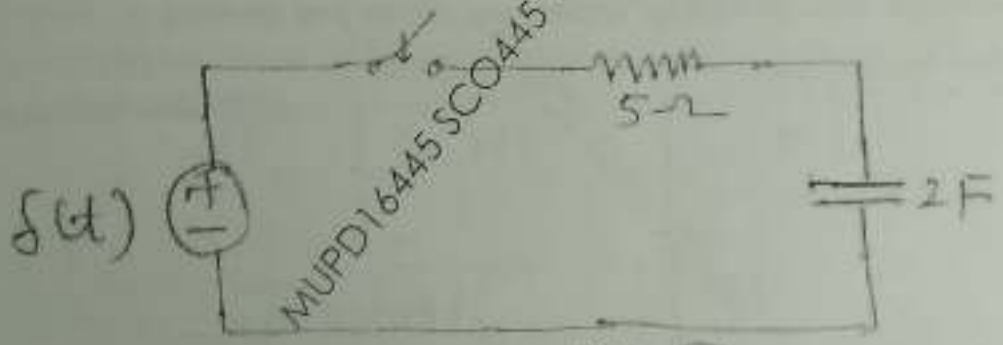
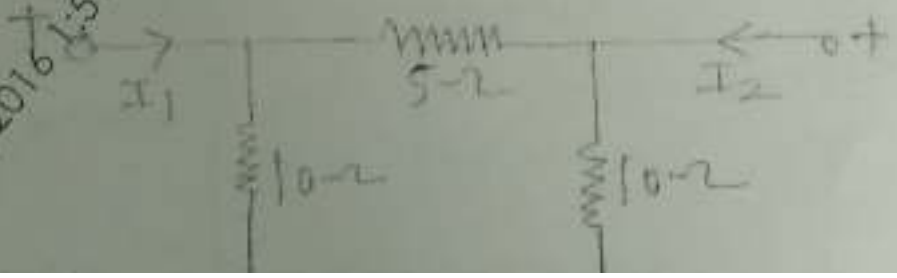


Fig (2)

(c) Find the lattice equivalent of symmetric π-network shown in figure (3). 5



(d) Define the following parameters of transmission line. 5

(i) Input impedance
(ii) Characteristics impedance
(iii) VSWR
(iv) Reflection coefficient
(v) Transmission coefficient

2. (a) In the network shown in fig. (4) the switch closes at t = 0. The capacitor has no initial charge. Find $V_c(t)$ and $i_c(t)$. 10

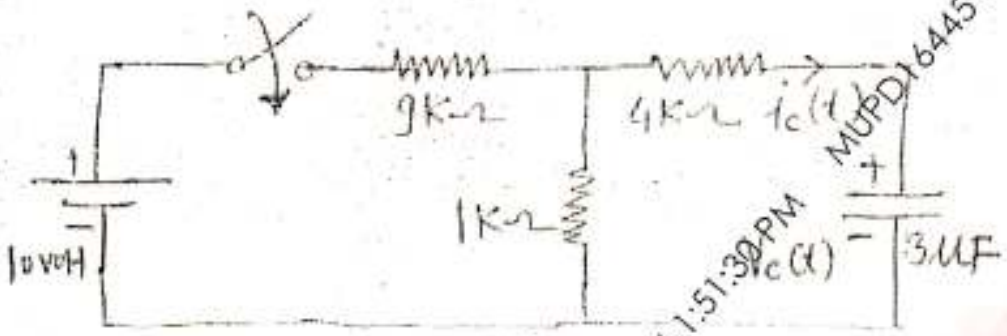


Fig (4)

(b) Determine the transmission parameters of the network shown in fig (5) using the concept of inter connection of two port network. 10

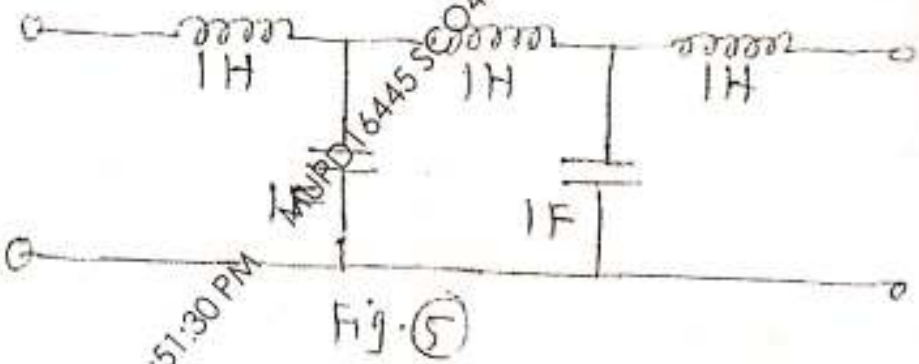


Fig. (5)

3. (a) For the network shown in fig (6), calculate the maximum power that may be dissipated in the load resistor R_L. **10**

(b) A load impedance $Z_L = (30 + j60)\Omega$ is connected to a 50Ω transmission line of 2 cm length and operated at 2 GHz. Using Smith Chart, find the imput impedance of transmission line under the assumption that phase velocity is 50% of speed of light. **10**

4. (a) An impedance is given by- **10**

$$Z(s) = \frac{8(s^2+1)(s^2+3)}{s(s^2+2)(s^2+4)}$$

Realise the network in Foster-I and Cauer-I form

(b) In the coupled circuit of figure (7), find the input impedance as well as the net inductance. **10**

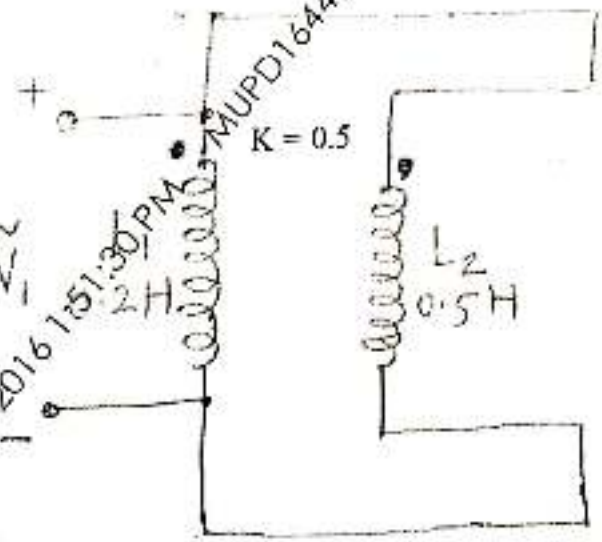
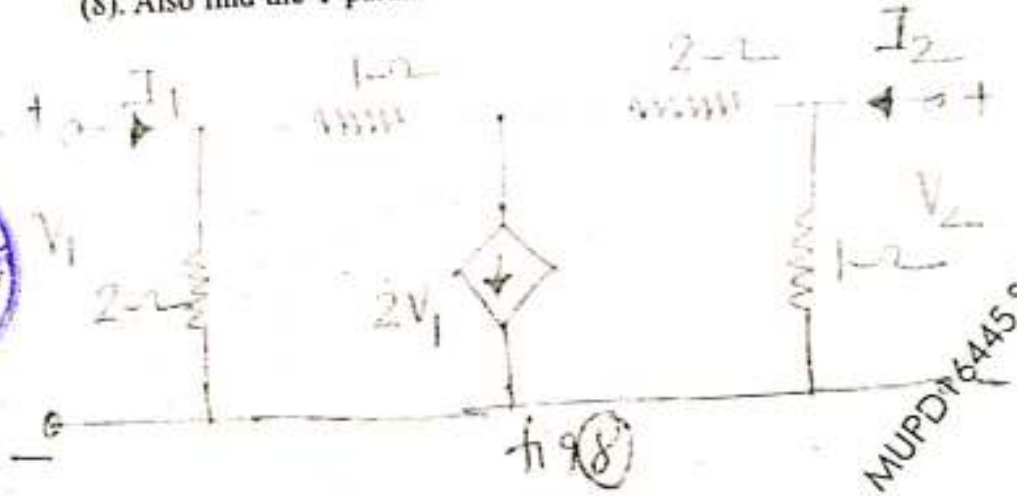


Fig (7)

5. (a) Find the open circuit impedance parameters of the circuit shown in fig. (8). Also find the Y parameters. 10



(b) (i) State properties of LC driving point impedance functions. 5

(ii) Test whether the polynomial is Hurwitz 5

$P(s) = s^7 + 2s^6 + 2s^5 + s^4 + 4s^3 + 8s^2 + 8s + 4$

6. (a) A co-axial line has the following parameters 10

$R = 6\ \Omega/m$

$L = 5.2 \times 10^{-8}$ H/m

$G = 6 \times 10^{-3}$ mho/m

$C = 2.136 \times 10^{-10}$ F/m

$f = 1$ GHz

$Z_L = (100 + j\ 100)\Omega$

Compute the following parameter using formulaes

(i) Characteristics impedance

(ii) Propagation constant

(iii) Reflection coefficient at the load

(iv) Transmission coefficient at the load

(b) In the network shown in fig (9), the switch is closed at t = 0. Find the current $i_1(t)$ and $i_2(t)$ when initial current through the inductor is zero and initial voltage is 4 volt. 10

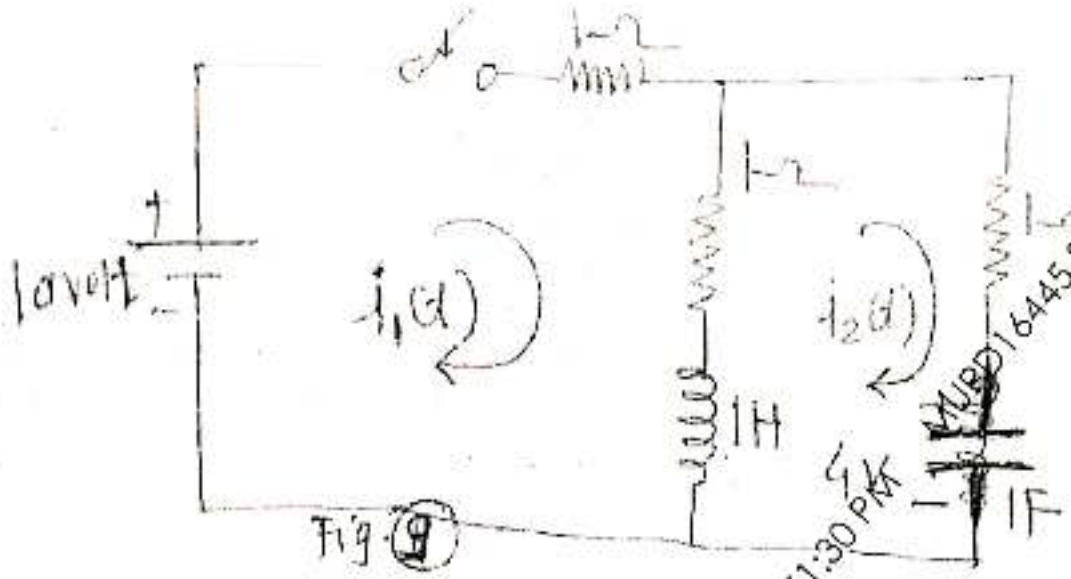


Fig (9)

BE PEM - III EXTC (CBSGS)

EI & M / EXTC / III / CBSGS

16-12-2016

Sub :- EI & M

Q.P. Code : 545500

(3 Hours) **[Total Marks : 80**

N.B. : (1) Attempt **four** questions, question no **1** is **compulsory**.
(2) Assume suitable data where ever required.
(3) Answers to the questions should be grouped together.
(4) Figure to the **right** of question indicates **full** marks.

1. Attempt any **four** : **20**
   (a) Significance of three and half digit display
   (b) Define accuracy, precision and sensitivity with suitable example
   (c) Explain working of strain gauge and its application in load measurement
   (d) List various sensors for pressure and temperature along with their ranges
   (e) A galvanometer, with a 1 mA full scale deflection and an internal resistance of 500Ω, is to be used as voltmeter, find series resistance for 1v and 10 v ranges.

2. (a) Draw and explain working of capacitive transducer for level measurement. **10**
   (b) Draw neat block diagram of CRO and explain its functioning, comment on role of sweep in CRO. **10**

3. (a) Draw and explain R-2R ladder network DAC for 3 bits input taking suitable example. **10**
   (b) Explain Kelvin's double bridge and its application in very low resistance measurement. **10**

4. (a) Explain SAR OR Flash type ADC with the help of block diagram and comment on its speed. **10**
   (b) Explain LVDT and define its application in displacement measurement. **10**

5. (a) Explain Hetrodyne type waves analyser and its applications. **10**
   (b) Discuss DSO with the help of block diagram along with various modes of operation also explain its applications. **10**

6. (a) Draw and discuss Hey Bridge and its application for measurement of inductance. **10**
   (b) Define power and energy and explain working of an energy meter. **10**

BE SEM – III EXTC (CBGS) NOV-DEC-2016

DE / EXTC / III / CBGS

09-12-16

Sub:- DE

Q.P. Code : 545401

(3 Hours) **[Total Marks : 80**

N.B. : (1) **Question No. 1** is compulsory.
(2) **Attempt any 3** questions from Q.2 to Q.6.
(3) Figures to the **right** in the bracket indicate **full** marks.
(4) Assume suitable data if necessary.

1.	a)	State basic theorems of Boolean algebra.	**5**
	b)	Compare Mealy and Moore machine	**5**
	c)	Define Noise Margin, Propagation delay, Power Dissipation	**5**
	d)	Design a full adder using half adders and logic Gates	**5**
2.	a)	Prove that NAND and NOR Gates are universal Gates	**10**
	b)	Design a 2-bit comparator and implement using logic Gates	**10**
3.	a)	Design a 4 bit Binary to Grey code converter.	**10**
	b)	Implement the given function using single 4:1 Multiplexer and few logic gates: $F(A, B, C, D) = \Sigma m(0, 1, 2, 4, 5, 6, 8, 9, 10, 12, 13, 15)$	**10**
4.	a)	What is a universal shift register? Explain its various modes of operation	**10**
	b)	Write a VHDL program to design a 3:8 Decoder.	**10**
5.	a)	Minimize the following expression using Quine McClusky Technique $F(A,B,C,D) = \Sigma m(0,1,2,3,5,7,9,11)$	**10**
	b)	Convert JK FF to T FF and JK FF to D FF	**10**
6.	a)	Explain the working of 3-bit asynchronous counter with proper timing diagram.	**10**
	b)	Write a note on CPLDs.	**10**

BE SEM - III EXTC (Old) Nov-Dec 2016
DLP / EXTC / III / DLP (Old)
09-12-16

Sub - DLD

QP Code : 544401

(3 Hours) [Total Marks : 100

N.B. : (1) Question **No. 1** is **compulsory.**
(2) Solve any **four** questions out of remaining **six.**
(3) Each question carries **20** Marks. Equal marks for the subquestions.
(4) Assume suitable data if required.

1. (a) Explain Minterm and Maxterm
   (b) Explain set, Reset, Preset and clear related to Flip-flops.
   (c) Explain various characteristics of logic families.
   (d) Explain various Binary codes with examples.

2. (a) State and Prove DeMorgan's theorems.
   (b) Design Full Adder using Logic gates.

3. (a) Minimize the following logical function using K-map.
   $f(A,B,C,D) = \pi M(4,5,6,7,8,12) \cdot d(1,2,3,9,11,14)$
   (b) Design 3 bit binary up Ripple counter using MS-JK Flip Flops and explain its working with output waveforms.

4. (a) Explain TTL Logic family.
   (b) Minimize the following logical function using Quine-McCluskey method.
   $f(A,B,C,D) = \Sigma_m (0,1,3,7,8,9,13,15)$

5. (a) (i) Design Y= A+BC using NAND gates only.
   (ii) Convert D-Flip-flop into T- FlipFlop.
   (b) Design 3-bit Binary code to Gray code converter using a Decoder with few gates.

6. (a) Design 16:1 Multiplexer using all 4:1 Multiplexers.
   (b) With neat sketch draw and explain the working of 3-bit SISO Register with output waveforms.

7. Write short notes on any **four** of the following :-
   (i) CMOS Logic family
   (ii) FPGA
   (iii) Number systems
   (iv) Asynchronous counter
   (v) PAL and PLA

A00-D | EXTC | III | CBGS

02-12-16

EXTC

Q. P. Code : 547400

DURATION: 3 HRS. **MAX. MARKS:80**

1) Question No. 1 is compulsory.
2) Attempt any THREE of the remaining.
3) Figures to the right indicate full marks.

Q 1.A) Determine the constants a, b, c, d, e if

$f(z) = (ax^4 + bx^2y^2 + cy^4 + dx^2 - 2y^2) + i(4x^3y - exy^3 + 4xy)$ is analytic. (5)

B) Find half range Fourier sine series for $f(x) = x^2, \quad 0 < x < 3$. (5)

C) Find the directional derivative of $\varphi(x,y,z) = xy^2 + yz^3$ at the point (2,-1,1) in the direction of the vector i + 2j + 2k. (5)

D) Evaluate $\int_0^{\infty} e^{-2t} t^5 \cosh t \ dt$. (5)

Q.2) A) Prove that $J_{\frac{3}{2}}(x) = \sqrt{\frac{2}{\pi x}}\left(\frac{\sin x}{x} - \cos x\right)$ (6)

B) If f(z) = u + iv is analytic and $u - v = e^x(\cos y - \sin y)$, find f(z) in terms of z. (6)

C) Obtain Fourier series for $f(x) = x + \frac{\pi}{2} \quad -\pi < x < 0$

$\frac{\pi}{2} - x \quad 0 < x < \pi$

Hence deduce that $\frac{\pi^2}{8} = \frac{1}{1^2} + \frac{1}{3^2} + \frac{1}{5^2} + \ldots$ (8)

Q.3) A) Show that $\bar{F} = (2xy + z^3)i + x^2j + 3xz^2k$, is a conservative field. Find its scalar potential and also find the work done by the force $\bar{F}$ in moving a particle from (1,-2,1) to (3,1,4). (6)

B) Show that the set of functions $\{\sin(2n+1)x\}, n = 0,1,2,\ldots$ is orthogonal over $[0, \pi/2]$. Hence construct orthonormal set of functions. (6)

[TURN OVER]

C) Find (i) $L^{-1}\{\cot^{-1}(s+1)\}$

(ii) $L^{-1}\left(\frac{e^{-2s}}{s^2+8s+25}\right)$ (8)

Q.4) A) Prove that $\int J_3(x)\,dx = -\frac{2J_1(x)}{x} - J_2(x)$ (6)

B) Find inverse Laplace of $\frac{s}{(s^2+a^2)(s^2+b^2)}$ $(a \neq b)$ using Convolution theorem. (6)

C) Expand $f(x) = xsinx$ in the interval $0 \leq x \leq 2\pi$ as a Fourier series.

Hence, deduce that $\sum_{n=2}^{\infty} \frac{1}{n^2-1} = \frac{3}{4}$ (8)

Q.5) A) Using Gauss Divergence theorem evaluate $\iint_S \bar{N}.\bar{F}\,ds$ where $\bar{F} = x^2i + zj + yzk$ and S is the cube bounded by x = 0, x = 1, y = 0, y = 1, z = 0, z = 1 (6)

B) Prove that $J_2'(x) = \left(1 - \frac{4}{x^2}\right)J_1(x) + \frac{2}{x}J_0(x)$ (6)

C) Solve $(D^2+3D+2)y = 2(t^2 + t + 1)$, with y(0)= 2 and y'(0)= 0 by using Laplace transform (8)

Q.6) A) Evaluate by Green's theorem for $\int_c (e^{-x}siny\,dx + e^{-x}cosy\,dy)$ where C is the the rectangle whose vertices are $(0,0), (\pi, 0), (\pi, \pi/2)$ and $(0, \pi/2)$ (6)

B) Show that under the transformation $w = \frac{z-i}{z+i}$, real axis in the z-plane is mapped onto the circle $|w| = 1$ (6)

C) Find Fourier Sine integral representation for $f(x) = \frac{e^{-ax}}{x}$ (8)

---X---X---X---

SE sem - III (old) Nov-Dec-16

Sub:- EDC-I

2/12/16

EXTC

Q.P. Code : 544300

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question **No.1** and **No.2** are **compulsory.**
(2) Answer **any three** questions from remaining questions.
(3) **Figures** to the **right** indicate **full marks.**
(4) Assume suitable **data** if **required.**

1. Design single stage RC coupled C E amplifier for following specifications: **20**
$A_v \geq 160$, $V_{CEQ} = 6.5V$, $I_{CQ} = 2.5mA$, $F_L = 20$ Hz. Use $V_{CC} = 15V$. Determine voltage gain, input impedance, output impedance.

2. Design single stage CS amplifier employing JFET type BFW11 for the following specifications : $A_v \geq 15$, $I_{DQ} = \frac{I_{DSS}}{5} mA$, $V_{CC} = 21V$ and $F_L = 20Hz$. Determine voltage gain, input impedance, output impedance. **20**

3. (a) Design fixed bias circuit with emitter resistance for $I_{CQ} = 1.2mA$, $V_{CE} = 5V$, $V_E = 1.5V$ and $\beta = 60$. Assume $V_{CC} = 9V$. Also derive the expression for stability factor for the above bias circuit. **10**
(b) Draw small signal hybrid parameter equivalent circuit for CB amplifier and define the same. What are the advantages of *h*-parameters? **10**

4. (a) For the amplifier shown in figure.1 analyze and determine : **10**
(i) I_{CQ}, V_{CEQ}, V_C, V_E
(ii) Small-signal voltage gain
(iii) Input and output impedance
The circuit parameters are :
$R_1 = 56k\Omega$, $R_2 = 12.2k\Omega$, $R_E = 0.4k\Omega$, $R_C = 2k\Omega$, $R_L = 10k\Omega$, $R_s = 0.5k$, $V_{CC} = 10V$ and BJT parameters are $\beta = 100$, $V_{BE} = 0.7V$.

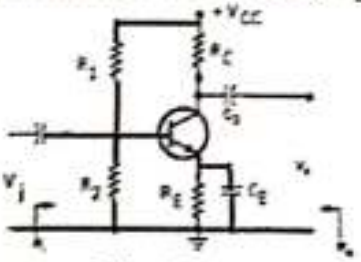


Fig. 1

TURN OVER

(b) Draw circuit diagram of JFET small signal Common Source amplifier (with any biasing) and derive the expression for, small signal mid-band voltage gain, input impedance and output impedance. **10**

5. (a) Explain the biasing techniques for D-MOSFET and E-MOSFET. **10**

(b) Design voltage divider biasing JFET for the following parameters : **10**

$I_{DSS} = 4mA$, $V_p = -2V$.

The circuit parameters :

$R_D = 1k\Omega$, $R_1 = 12M\Omega$, $I_{DQ} = 3.4mA$, and $V_{DS} = 10.5V$, $V_{DD} = 21V$.

6. (a) What is bleeder resistance? **10**

Design L section LC filter with full wave rectifier to meet following specifications : The DC output voltage $V_{DC} = 200V$, deliver $I_L = 50mA \pm 20mA$ to the resistive load, and required ripple factor is 0.04.

(b) Design a simple Zener voltage regulator to meet the following specifications: **10**

Output voltage $V_0 = 6.2V$, Load current $I_{Lmax} = 50mA$, $I_{Lmin} = 0.1mA$, $I_{zmax} = 90mA$, $I_{zmin} = 5mA$, $P_Z = 420mW$ and Input voltage $V_i = 20V$ to 30V.

7. Write short notes on following (**any two**) : **20**

(a) Construction and Characteristics of SCR

(b) Diode compensation for I_{CO} techniques

(c) Construction and Characteristics of E-MOSFET

Transistor type	P_{tot} max. @ 25°C Watts	I_{Cmax} @ 25°C Amps	V_{CE} volts d.c.	V_{CBO} volts d.c.	V_{CEO} (Sus) volts d.c.	V_{CER} (Sus) volts d.c.	V_{CEX} (Sus) volts d.c.	V_{CEX} volts d.c.	V_{EBO} volts d.c.	T_j max °C	D.C. current gain min.	typ.	max.	Small - Signal h_{fe} min.	typ.	h_{fe} max.	V_{BE} max.	θ_{j-c} °/W	Derate above 25°C W/°C
2N 3055	115·5	15·0	1·1	100	60	70	90	7	200	20	50	70	15	50	120	1·8	1·5	0·7
ECN 055	50·0	5·0	1·0	60	50	55	60	5	200	25	50	100	25	75	125	1·5	3·5	0·4
ECN 149	30·0	4·0	1·0	80	40	—	—	8	150	30	50	110	33	60	115	1·2	4·0	0·3
ECN 100	5·0	0·7	0·6	100	60	65	—	6	200	50	90	280	50	90	280	0·9	25	0·03
BC147A	0·25	0·1	0·25	50	45	50	—	6	175	115	180	220	125	220	260	0·9	—	—
2N 525(PNP)	0·225	0·5	0·35	85	80	—	—	—	100	35	—	65	—	45	—	—	—	—
BC147B	0·25	0·1	0·25	50	45	50	—	6	125	200	290	450	240	330	500	0·9	—	—

Transistor type	h_{fe}	h_{oe}	h_{re}	θ_{j-c}
BC 147A	2·7 K Ω	18μ Ʊ	$1·5 \times 10^{-4}$	0·4°C/mW
2N 525 (PNP)	1·4 K Ω	25μ Ʊ	$3·2 \times 10^{-4}$	—
BC 147B	4·5 K Ω	30μ Ʊ	2×10^{-4}	0·4°C/mW
ECN 100	500 Ω	—	—	—
ECN 149	250 Ω	—	—	—
ECN 055	100 Ω	—	—	—
2N 3055	25 Ω	—	—	—

BFW 11—JFET MUTUAL CHARACTERISTICS

–Vgs (volts)	0·0	0·2	0·4	0·6	0·8	1·0	1·2	1·6	2·0	2·4	2·8	3·2	4·0
Ids max. mA	10	9·0	8·3	7·6	6·8	6·1	5·4	4·2	3·1	2·2	2·0	1·1	0·3	0·0
Ids typ. mA	7·0	6·0	5·4	4·6	4·0	3·3	2·7	1·7	0·8	0·2	0·0	0·0	0·0	0·0
Ids min. mA	4·0	3·0	2·3	1·6	1·0	0·5	0·0	0·0	0·0	0·0	0·0	0·0	0·0	0·0

N-Channel JFET

Type	V_{ds} max. Volts	V_{gs} max. Volts	V_{gd} max. Volts	P_d max. @25°C	T_j max.	I_{dss}	C_{iss} (typical)	$-V_p$ Volts	r_d	Derate above 25°C	θ_{j-c}
2N5432	30	30	30	300 mW	175°C	2 mA	3000 μ Ω	6	50 KΩ	2 mW/°C	0·5°C/mW
BFW 11 (typical)	30	30	30	300 mW	200°C	7 mA	3600 μ Ω	3·5	50 KΩ	—	0·3° C/mW

SE SEM-III / EXTC / AE-I / CBGS

25/11/16

NOV - DEC -2016

EXTC SE SEM - III CBGS

Sub - AE - I

QP Code : 545201

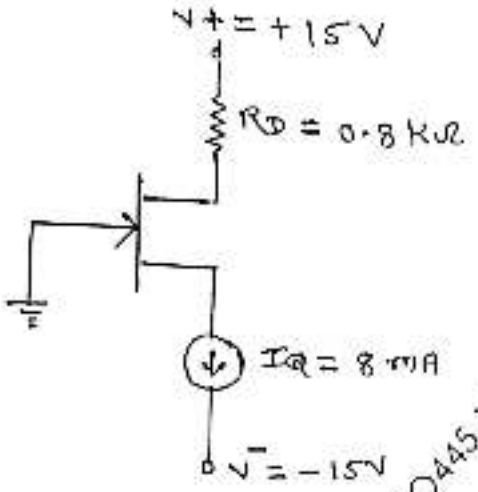
(3 Hours)

[Total Marks : 80

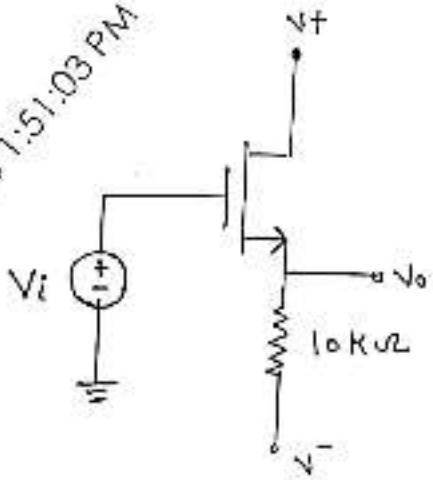
N.B. : (1) Question **No. 1** is **compulsory.**
(2) Attempt **any three** questions out of remaining five questions.
(3) Assume suitable data if required and mention the same in answer sheet.

1. Attempt **any five** questions **20**

(a) For the circuit given below, the transistor parameters are Vp = -3.5V, I_{DSS} =18mA and λ=0. Calculate V_{GS} and V_{DS}.



(b) The small -signal parameters of the NMOS transistor in the source follower circuit shown in fig. below are gm=5mA/v and ro = 100 KΩ. Determine the voltage gain and output resistance.



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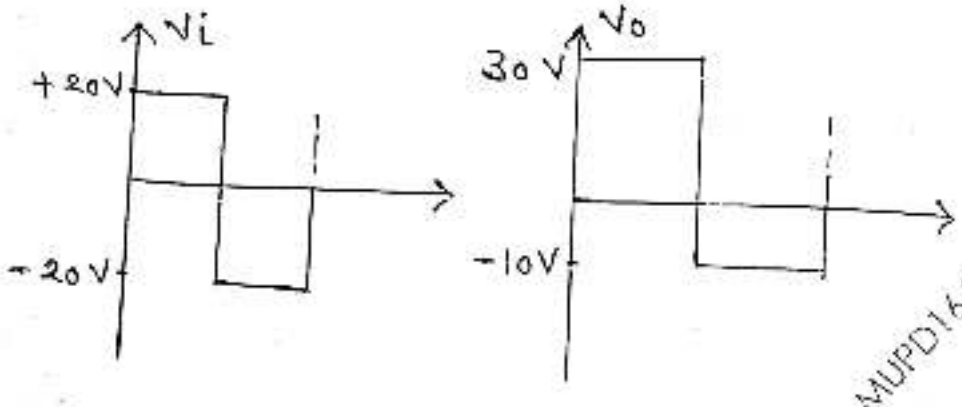
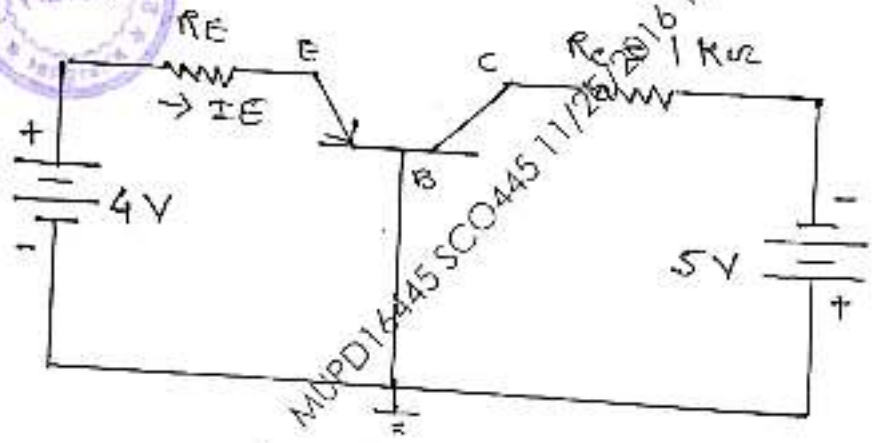
(c) Design a diode clamper to generate a steady-State output voltage Vo from the input voltage Vi in fig. Shown below if diode is Ideal.



(d) For the circuit shown, determine R_E such that the emitter current is limited to I_E =1mA, Also find I_B (Given $\alpha = 0.992$)



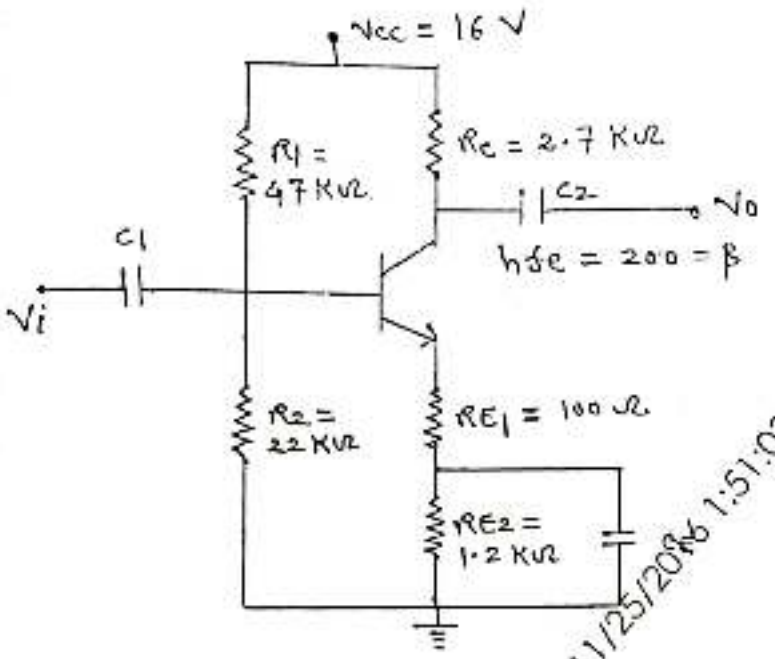
(e) Describe the channel length modulation effect and define the parameters.

(f) Draw a neat circuit diagram of emitter follwer configuration and its hybrid-π model.

2 (a) Determine the following for the network given below 10

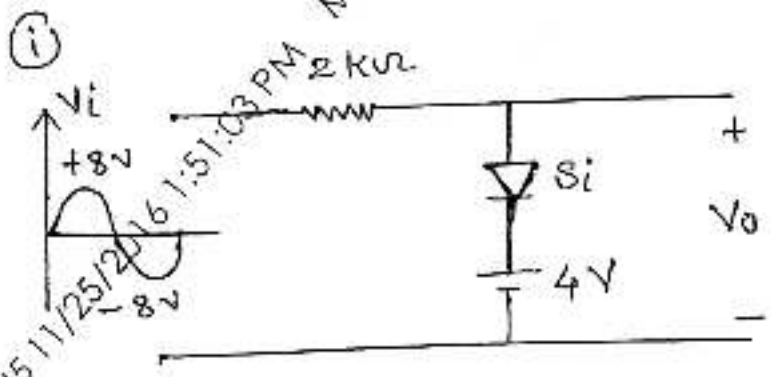
(i) Q- Point

(ii) Av, Ai, Zi, Zo.

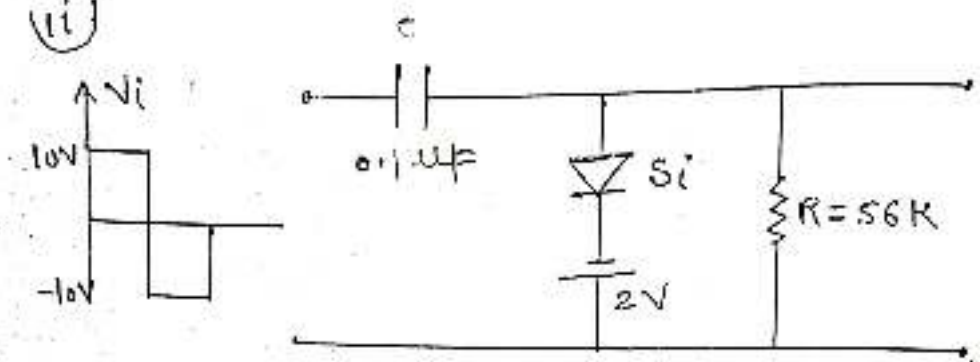


(b) Explain the working of Wein Bridge oscillator. Derive the expression for frequency of oscillation and condition of oscillation. 10

3 (a) Draw output waveform for clipper and clamper circuits shown. 10

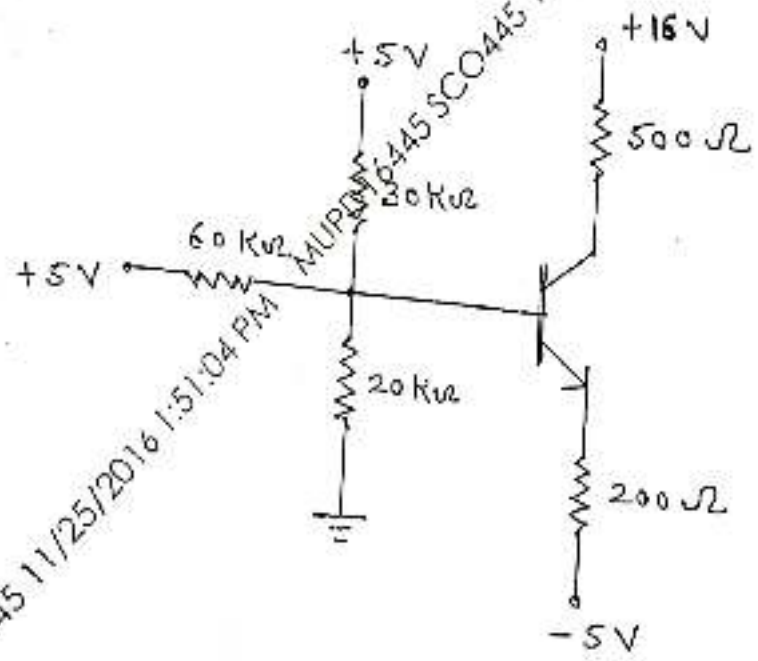


(ii)



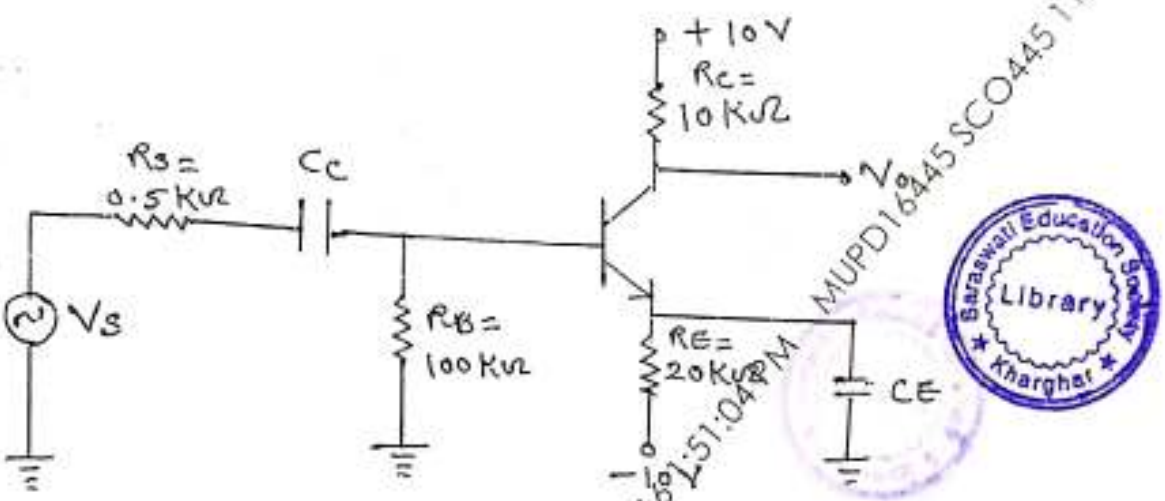
(b) Explain construction and characteristics of n-channel Depletion MOSFET. Draw transfer characteristics and drain characteristics. 10

4 (a) Find I_{CQ} and V_{CEQ} for the circuit shown in figure if $\beta = 100$ 10



5

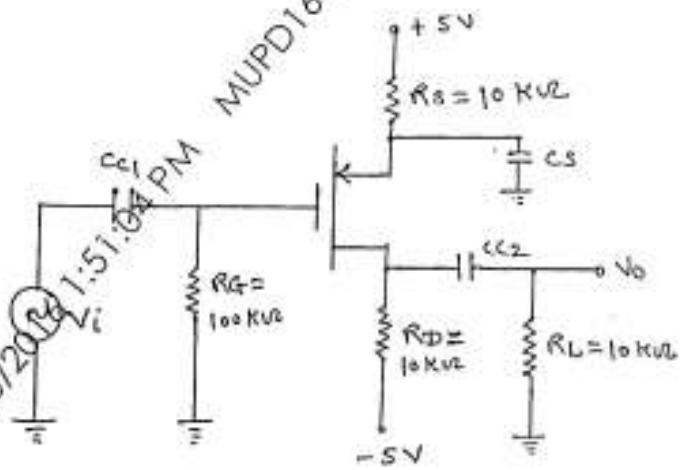
(b) For the circuit in fig. let β =100, VA=100V, VBE (on) = 0.7V. Determine (i) Small signal voltage gain (ii) Input resistance seen by the signal source (iii) output resistance 10



5. (a) For the amplifier circuit shown below 10

(i) Determine the values of Kp such that V_{SDQ} =6V

(ii) Determine the resulting value of I_{DQ} and small signal voltage gain.



$V_{TP} = -2V$, $\lambda = 0$

[TURN OVER]

(b) Draw circuit diagram of common source amplifier with voltage divider bias with unbypassed source resistance 'Rs' using n-channel EMOSFET. Derive expression for voltage gain, input resistance and output resistance. 10

6. Write short note on **any four** :- 10

(i) Energy band diagram of MOS capacitor
(ii) Construction and operation of Schottky diode
(iii) Crystal Oscillator
(iv) Hybrid parameters
(v) Stability factor of biasing circuit.
