TE /SEM VI /CBSGS/ EXTC / DC / 14/05/2018

Q. P. Code : 38833

(3 Hours) (Total Marks : 80

N.B. 1. **Question No 1 is compulsory.**
2. Attempt any three questions out of remaining five.
3. All questions carry equal marks
4. Assume Suitable data, if required and state it clearly.

1 Attempt any **FOUR** [20]

1. With a relevant block diagram, explain duobinary signalling scheme. Why is it called correlative coding? Write the output for bitstream 001100.
2. What is DBPSK? What advantage does it have over conventional PSK?
3. Show the entropy is maximum when all the symbols of a discrete memoryless source are equiprobable.
4. Why are line codes necessary? What are the different parameters which need to be examined before choosing a PCM waveform for a particular application?
5. Contrast and Compare systematic and non-systematic block codes.

2 a Consider an alphabet of a discrete memoryless source having following source symbols with their respective probabilities as 0.40, 0.20, 0.12, 0.08, 0.08, 0.08, and 0.04. [10]
- i) Create a Huffman Tree following the standard algorithm for the Huffman encoding, and compute the codeword and respective length of the codewords for each of the given sources symbols.
- ii) Determine the average codeword length.
- iii) Determine entropy of the specified discrete memoryless source.
- iv) Determine the Coding efficiency

b Consider (3,1,2) convolution code with $g^{(1)}=100$, $g^{(2)}=101$ and $g^{(3)}=111$ [10]
- i. Draw the encoder for this code
- ii. Draw the state transition diagram
- iii. Using state transition diagram, find the codeword for the sequence 1101.
- iv. Derive the code transfer function.

3 a Explain 16-ary PSK with respect to the following terms:- [10]
1. Modulator and Demodulator
2. Power spectral density and Bandwidth.

b Consider a (7, 4) cyclic code generated by $g(x) = 1 + x^2 + x^3$. [10]
- i) Design an encoder for systematic cyclic code generation using shift registers
- ii) Using encoder implemented in (i) and not otherwise, find the code word for message (1001).
- iii) Suppose the received vector is R = (0 0 1 0 1 1 0), find the syndrome using syndrome circuit.
- iv) Find out the generator matrix for the above cyclic code.

4 a Draw the block diagram of QPSK Transmitter and receiver and Sketch the waveform and explain. [10]

b Explain Direct sequence spread spectrum (DS-SS) with neat diagram. Explain processing gain and Jamming Margin with necessary expressions. [10]

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5 a Consider a Systematic block code whose Parity check equations are: [10]

P1= m1 + m2 + m3 P2= m1 + m2 + m4

P3= m1 + m3 + m4 P4 = m2 + m3 + m4

Where mi are message bits and Pi are parity check bits. In a codeword parity bits appear before message bits.

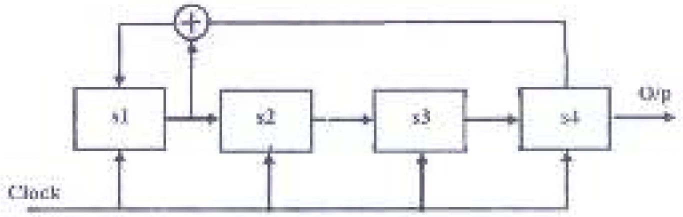
(i) Find Generator matrix (G) and Parity check matrix (H)

(ii) Find the code words for the message vectors: 1001, 1101

(iii) How many errors can the code correct and detect?

(iv) If the received code word is 10011101, decode the message.

b The following circuitry is used to generate PN sequence with initial content (Seed) as 1011. [10]



i. Write down the PN sequence.

ii. Verify the balance property of PN Sequence.

iii. Verify the Auto-correlation property of the PN sequence.

6 a What do you mean by eye diagram? What is its purpose? Mention the four parameters observed from the eye pattern. Explain it with help of suitable illustration. [10]

b Justify that the probability of error in matched filter does not depend on the shape of input signal. Derive the relevant expression. [10]

EXTC) CBSGS / Sem VI / DTSP / 18.5.18

Q.P. CODE: 37021

Time 3 hours **Marks: 80**

N.B: (1) Questions NO.1 is compulsory.
(2) Attempt any three questions out of remaining five questions.
(3) Assume suitable data if required.
(4) Figures to the right indicate full marks.

Q 1.Solve any four 20

a. Determine the zeros of the following systems and indicate whether the system is minimum, maximum or mixed phase.

1) $H_1(z) = 6+z^{-1}+6z^{-2}$
2) $H_2(z)= 1-z^{-1}-6z^{-2}$.

b. What is multirate DSP? State its applications

c. Compare BLT and impulse invariant method.

d. Explain concept of decimation by integer D.

e. If X(K)={16,-4,0,-4}, determine x[n] using IFFT.

Q 2. a) If x(n)={ 1,2,3,} and h(n)={1,0}

1) Find linear convolution using circular convolution.
2) Find circular convolution using DFT-IDFT. 10

b) Show the mapping from S plane to Z plane using impulse invariant method. Explain its limitations. Using this method determine H(z) if

$H(s)=\frac{2}{(s+1)(s+2)}$ if Ts=1s. 10

Q3. a) Compute DFT of sequence x(n)={ 1,2,3,4,5,6,7,8} using DIT-FFT algorithm. 10

b) Design low pass IIR Butterworth filter for following specifications

Passband attenuation =1dB

Stopband attenuation =40dB

Passband edge frequency=200Hz

Stopband edge frequency=540Hz

Sampling frequency=8KHz

Use Bilinear transformation method. 10

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Q 4. a) A low pass filter is to be designed with following desired frequency response.

$$H_d(e^{jw}) = e^{-j2w} \qquad -\frac{\pi}{4} \le w \le \frac{\pi}{4}$$

$$= 0 \qquad \frac{\pi}{4} < w \le \pi$$

Determine the filter coefficients $h_d(n)$ if the window function is defined as

$w(n)=1 \qquad 0 \le n \le 4$

$=0 \qquad$ otherwise

Also determine the frequency response $H(e^{jw})$ of the designed filter. 10

b) Find DFT of x(n)={1,2,3,4}. Using these results not otherwise find DFT

i) $x_1(n)=\{4,1,2,3\}$

ii) $x_2(n)=\{2,3,4,1\}$

iii) $x_3(n)=\{6,4,6,4\}$ 10

Q 5 a) Explain subband coding of speech signal as a application of multirate signal processing. 10

b) Determine the Direct form-I and Direct form-II realization for the system $y(n) = -0.1y(n-1) + 0.2y(n-2) + 3x(n) + 3.6x(n-1) + 0.6x(n-2)$. 10

Q6. Write Short note on

a) Dual Tone Multifrequency Detection using Goertzel's algorithm 07

b) The effects of coefficients quantization in FIR filters. 07

c) Concept of interpolation by integer factor I 06

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EXTC / sem VII / CCTN / CBSGS / 24-05-18

Q. P. Code : 13295

(3 Hours) **(Total Marks: 80**

N.B. :

(a) Question No.1 is compulsory.
(b) Total 4 questions need to be solved.
(c) Attempt any three questions from remaining five questions.
(d) Assume suitable data wherever necessary, justify the same.

1.a	What are the roles of sub layer of data link layer?	[4]
1.b	Define i) Load ii) Throughput How it will impact on network?	[4]
1.c	Explain Connection oriented protocol with example.	[4]
1.d	Explain the working principle of MPLS.	[4]
1.e	List the features of Link State Routing.	[4]
2.a	What are the roles of two level and three level switch? Justify router as an Intelligent device.	[8]
2.b	Compare between IPv4 to IPv6. Explain the concept of tunneling.	[6]
2.c	Derive the expression of efficiency of slotted ALOHA.	[6]
3.a	List the exclusive features of TDM.	[4]
3.b	Explain in detail the networking topologies and explain which is practically preferred.	[8]
3.c	List the use of Multiple Access Techniques and Explain the CSMA/CD.	[8]
4.a	BGP is Exterior Routing Protocols explain with working principle.	[8]
4.b	Define: i) Unicast ii) Any cast ii) Multicast. Explain with a suitable example.	[8]
4.c	Discuss the working Principle of Satellite Network.	[4]
5.a	What do you mean by Peer to Peer communication? Explain with respective protocol.	[8]
5.b	Compare between TCP and UDP and explain the UDP multiplexing and demultiplexing.	[8]
5.c	Explain the concept Network Socket Programming.	[4]
6	Write short notes on any two : (a) WiMAX (b) Physical media (c) DNS	[20]

EXTC / VI / CBSGS / TVE / 30.5.18 **Q. P. Code: 36266**

Time: 3 hours **Marks: 80**

Note:

- Question no 1 is compulsory
- Attempt any 3 questions out of remaining 5 questions each carrying 20 marks (Q2 – Q6) from all modules
- Illustrate answer with sketches and examples wherever required.

1. Answer **any 4** from the following: (20)
   a. Why (G-Y) is not transmitted in color television system?
   b. List electrical characteristics of NTSC system
   c. Channel bandwidth in PAL system is 7 MHz. Draw and explain
   d. Give reason – Cross color and cross luminance interference is eliminated in MAC signal transmissions
   e. Draw tuner block diagram in television receiver and explain the function
   f. State the following:
      i. Horizontal scanning frequency in PAL system
      ii. Vertical scanning frequency in PAL system
      iii. Picture IF
      iv. Sound IF

2. Draw PAL encoder block diagram and explain in detail. Also explain how phase errors get cancelled in PAL system (20)

3. Answer the following:
   a. Explain interlaced scanning in TV system in detail with appropriate diagrams and waveforms (10)
   b. Draw composite video signal and label all parts. Explain why sync pulses are above black level (10)

4. (a) Explain MAC encoding in digital TV system. Draw D2 MAC signal (10)
   (b) Explain DTH system (10)

5. Answer the following:
   a. Explain the working of LCD display (10)
   b. Explain why Chroma is subsampled in digital video formats. Give details of Rec 601 (4:2:2) (10)

6. Write short notes on: **(Any two)** (20)
   a. HDTV
   b. MUSE system
   c. Camera tubes (Any one)
   d. Compatibility considerations in monochrome and color TV

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EXTC/ sem VI / CBSGS/ OS/ 05/06/18

Q.P.Code: 38993

(3 Hours) [Total Marks: 80]

N.B. (1) Question No. 1 is compulsory
(2)Assume suitable data if necessary
(3)Attempt any three questions from remaining questions

1
(a) What is operating system? Explain different functions of OS. (5)
(b) Explain critical section problem. (5)
(c) Explain the concept of segmentation. (5)
(d) What are the characteristics of a Real Time OS? (5)

2 (a) Explain the process transition diagram for UNIX operating system. (10)
(b) Consider the following set of processes with CPU burst time given in milliseconds. (10)

Process	Burst time	Arrival time
P1	10	1
P2	4	2
P3	5	3
P4	3	4

Draw Gantt chart for FCFS and Shortest Remaining Time First(SRTF) and calculate average waiting time and average turnaround time.

3 (a) What is a deadlock? Explain the necessary and sufficient conditions for the deadlock. (10)
(b) Describe process management in LINUX. (10)

4 (a) Explain the working of EDF and RMA real time scheduling algorithms. (10)

(b) Calculate page hit and page miss for the following string using page replacement policies FIFO and LRU. Page frame size is 3. (10)
2,3,4,2,1,3,7,5,4,3,2,3,1

5 (a) Explain RAID with different levels. (10)
(b) Explain how UNIX performs file management using I-nodes. (10)

6 (a) What are system calls? Explain any five system calls. (10)
(b) What is semaphore? Give an implementation of bounded buffer producer consumer problem using semaphore. (10)

EXTC / sem VI / CBSGS / VLSI Design / 11/06/18

Q. P. Code: 36647

Duration: 3 Hours **Marks:80**

1] Question no.1 is **compulsory**
2] Attempt any **three** questions out of remaining questions
3] Assume **suitable data** if **required**

Q. No. 1) Attempt any four from the following [20]

a) Calculate the voltage at the output node V_o if V_{DD}=5V and V_{dl}=1.5V

b) Implement 2:1 multiplexer circuit using pass transistor logic and state its drawback. Draw the circuit using CMOS transmission gates.

c) State the conditions required for the symmetric static CMOS inverter.

d) Compare ion implantation with diffusion stating its advantages and disadvantages.

e) In 2-input CMOS NAND gate all PMOS transistors have (W/L)p = 20 and all NMOS transistors have (W/L)n = 10. Draw its equivalent CMOS inverter for simultaneous switching of all inputs and find size of PMOS and NMOS transistor in the equivalent inverter circuit.

Q. No. 2)

a) A CMOS inverter has following parameters

V_{DD} = 3.3V $V_{to,n}$ = 0.6V $V_{to,p}$ = -0.7V

K_n =200μA/V² Kp =80μA/V²

Calculate the noise margin of the circuit. Is the inverter symmetric? [10]

b) Implement $Y = \overline{A(B+C)+DE}$ [10]

(i) static CMOS logic
(ii) Dynamic logic
(iii) Depletion load logic
(iv) Pseudo NMOS logic

Q. No. 3)

a) Explain in detail the fabrication sequence of PMOS transistor with cross sectional view of each step. [10]

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b) Draw schematic and layout diagram of six transistor SRAM cell and explain Read and write operations. [10]

Q. No. 4)

a) Compare constant field scaling with constant voltage scaling and state advantages and limitations in both the methods. Show the effect of scaling on power density and current density. [10]

b) Design a 3- bit carry generator block of carry look ahead adder using multiple output domino logic (MODL) style. Explain how it achieves better speed compared to ripple carry adder. [10]

Q. No. 5)

a) Draw layout diagram of two input CMOS NAND gate using lambda design Rules with $(L/W)_p=1/2$ and $(L/W)_n=2/1$. (Indicate scale in terms of lambda on layout). [10]

b) Draw transistor level CMOS negative edge triggered master slave D flip flop. [5]

c) What are the limitations of single phase clock? Explain with neat diagram two phase clock system. [5]

Q. No. 6) Write short notes on any four [20]

i) ESD protection circuit.
ii) 4x4 Barrel shifter
iii) MOSFET Capacitances
iv) Design rules and their necessity
v) Clock skew and clock jitter

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